Attorney Docket 920522-905337

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TO: **Commissioner for Patents**

EXAMINER: **Eugene Lee**

GROUP ART UNIT: **2815**

Attached: Response to Office Action Dated April 8, 2005

If you do not receive all pages, please contact William M. Lee, Jr. at (312) 214-4800 or his assistant, Minnie Wilson at (312) 214-4829.

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Minnie Wilson
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Signature

July 8, 2005

CHDS01 WLEE 236803v1

920522-905337

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE THE APPLICATION OF

Bart Dieriekx

SERIAL NO.: 09/736,651

FILED: December 13, 2000

FOR: A Pixel Structure with Improved Charge Transfer

Examiner: Eugene Lee

Group Art Unit: 2815

Customer number: 23644

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Name of person signing Minnie Wilson
Signature Minnie Wilson

RESPONSE TO OFFICE ACTION DATED APRIL 8, 2005

Honorable Director of Patents and Trademarks
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This response is being filed in view of the Examiner's further Office Action of April 8, 2005. No amendments are being offered, as none are believed to be appropriate as will be discussed in greater detail below.

* * *

With respect to the objection to claim 1 (typographical error in line 11), the Applicant respectfully submits that there does not seem to be a typographical error. The amendment in lines 10 and 11 of claim 1, entered with the submission of 15 February 2005, says that "the region [...] is substrate under a [...] gate electrode". No typographical error has been made, and it is requested that this objection be withdrawn.

* * *

Claim 1 is still rejected under 35 U.S.C. §102(e) as being anticipated by Rhodes. The Examiner includes in his rejection the following drawing:

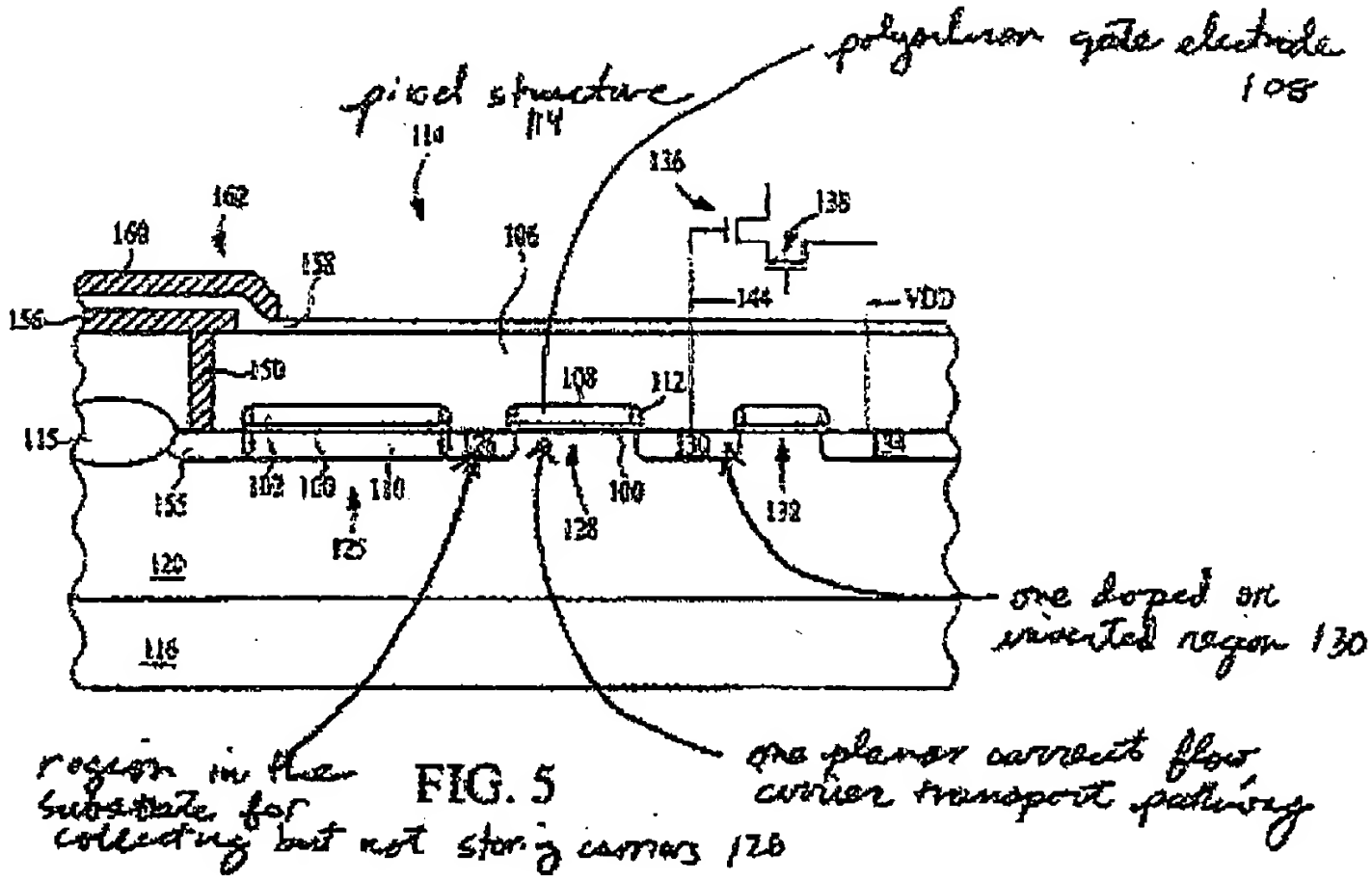
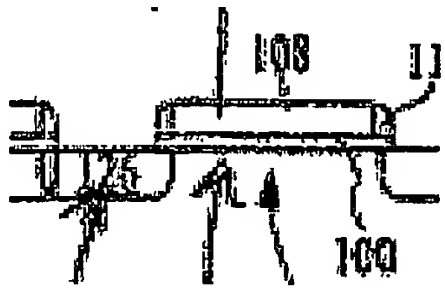


FIG. 5

If, in view of the mistakenly mentioned dopant concentration levels in the present patent application, region 126 of Rhodes is considered a region for collecting but not storing carriers as in the present patent application, then still Rhodes does not disclose all features of claim 1 as presently on file, as it does not disclose that the region for collecting but not storing carriers is substrate under a polysilicon gate. This can be clearly seen in the above drawing, reference number 126 indicating the region for collecting but not storing carriers, and reference number 108 indicating the polysilicon gate electrode.

If the Examiner would refer consider there being a slight overlap between region 126 and gate electrode 108, it is submitted that this is not true, as shown in the enlarged portion of the above drawing reproduced hereinbelow:



The Applicant submits that there is no overlap between the region 126 and the electrode 108, but rather between the region 126 and a spacer next to the electrode 108. Application of spacers is commonly known in semiconductor processing, and is used in order to align features. No portion of the polysilicon gate electrode 108 is present above region 126.

The substrate under the gate electrode 108 in Rhodes is not a region for collecting carriers, in view of the presence of highly doped region 126, which will collect charges generated in the substrate.

The applicant has previously explicitly elected the embodiment corresponding to Fig. 10a and Fig. 10b, this embodiment not having a competition between substrate and a first conductivity type region for collecting charge carriers. This way only substrate under a gate electrode is left for collecting carriers. The second conductivity type regions 8 illustrated in Fig. 10a of the present patent application (p-well implant) will not collect any charges in view of their dopant type. Therefore, the only place where charges can be collected in accordance with the present invention is in the substrate under the polysilicon gate electrode.

As can be seen from the above argumentation, there is a significant difference between Rhodes and the present patent application in that Rhodes does not comprise a carrier collecting non carrier storing region which is substrate under a polysilicon gate electrode. Rhodes does not hint in the direction of applying such region, and neither does any of the other cited prior art documents. Therefore, claim 1 is considered novel and non-obvious in view of the cited prior art, and thus allowable thereover.

Claims 7 to 10 are also considered to be allowable, in view of their dependency on claim 1

* * *

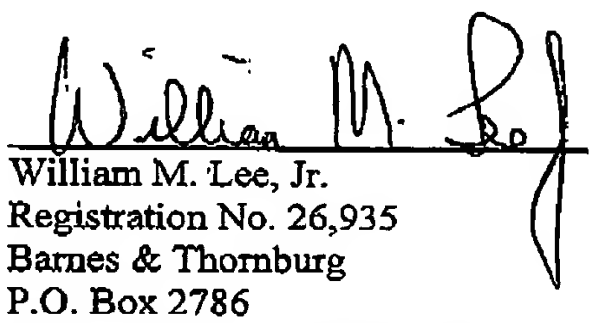
Reconsideration of the application is requested in view of the above arguments. The Applicant would like to request that the Examiner contact the undersigned for an interview before issuing any futher action if he deems the present patent application still not to be in a condition for allowance.

* * *

Further and favorable reconsideration of the application is therefore urged.

July 8, 2005

Respectfully submitted



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